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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/197,993	11/23/1998	STEVEN EUGENE LOVETTE		1952

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EXAMINER

NGUYEN, DUSTIN

ART UNIT PAPER NUMBER

2154

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/197,993	Applicant(s) LOVETTE, STEVEN EUGENE	
	Examiner Dustin Nguyen	Art Unit 2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 June 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 26 – 49 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/19/2006 has been entered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 26-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following terms lack antecedent basis:

- I. the value - claims 26 and 38.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 26-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta [US Patent No 5,222,220], in view of Hastings [US Patent No 5,535,329].

7. As per claim 26, Mehta discloses the invention substantially as claimed including a method for detecting corruption associated with a stack in storage device, the stack encompassing a range of memory of a fixed size, the method comprising the steps of:

detecting the occurrence of a stack operation within the stack [i.e. detecting subroutine or interrupt logic [jump, branch]] [col 3, lines 12-21 and lines 49-54]; and

comparing the value in the first address location to the first predetermined value to determine if the stack operation corrupted the first predetermined value stored in the first address location [i.e. the return address is compared with the address in the return address latch register] [48, Figure 3; Abstract; col 3, lines 59-col 4, lines 17; and col 5, lines 38-col 6, lines 10].

Mehta does not specifically disclose

storing a first predetermined value in a first address location immediately preceding the range of memory.

Hastings discloses

storing a first predetermined value in a first address location immediately preceding the range of memory [i.e. allocate 8 bytes of memory before and after each array] [Abstract; and col 11, lines 41-67].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Hastings because Hastings' teaching of allocating memory before and after each array would allow to detect array bounds violations and similar data errors [Hastings, col 11, lines 44-46].

8. As per claim 27, Mehta discloses the first determined value comprises a known bit pattern [i.e. store address in a latch register] [40, Figure 3; and col 3, lines 41-45].

9. As per claim 28, Mehta discloses wherein the first predetermined value comprises a processor readable address [i.e. return address] [Abstract; and col 3, lines 41-45].

10. As per claim 29, Mehta does not disclose wherein the first predetermined value comprises a processor readable instruction. Hastings discloses wherein the first predetermined value comprises a processor readable instruction [i.e. watchpoint] [col 8, lines 50-55; and col 12, lines 20-30]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Hastings because Hastings' teaching of watchpoints would allow to perform a more comprehensive monitoring of array bound violations [Hastings, col 11, lines 41-50].

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11. As per claim 30, Mehta does not specifically disclose wherein the stack operation inserts data in the stack. Hastings discloses wherein the stack operation inserts data in the stack [i.e. push on stack] [Figure 10; and col 12, lines 51-53]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Hastings because Hastings' teaching of push data on stack would allow data to be retrieved in orderly manner at a later time to prevent the out-of-order processing and prevent system corruption.

12. As per claim 31, Mehta does not specifically disclose wherein the stack operation removes data from the stack. Hastings discloses wherein the stack operations removes data from the stack [i.e. reclaiming stack space] [col 10, lines 33-35]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Hastings because Hastings' teaching of reclaiming stack space would allow to save memory space so that memory space can be utilized for other purposes.

13. As per claim 32, Mehta does not specifically disclose the step of storing a second predetermined value in a second address location immediately following the ending location of the stack. Hastings discloses the step of storing a second predetermined value in a second address location immediately following the ending location of the stack [i.e. allocate 8 bytes of memory before and after each array] [Abstract; and col 11, lines 41-67]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mehta and Hastings because Hastings' teaching of allocating memory before and after each array

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would allow to detect array bounds violations and similar data errors [Hastings, col 11, lines 44-46].

14. As per claims 33-37, they are rejected for similar reasons as stated above in claims 27-31.

15. As per claim 38, it is apparatus claimed of claim 26, it is rejected for similar reasons as stated above in claim 26. Furthermore, Mehta discloses the stack encompassing a range of memory of a fixed size [i.e. reserve area of memory] [col 2, lines 67-col 3, lines 2].

16. As per claims 39-49, they are apparatus claimed of claims 27-37, they are rejected for similar reasons as stated above in claims 27-37.

17. Applicant's arguments with respect to claims 26-49 have been considered but are moot in view of the new ground(s) of rejection.

18. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dustin Nguyen
Examiner
Art Unit 2154

A handwritten signature in black ink, appearing to read 'Dustin', with a long horizontal flourish extending to the right.